BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Your search matched **12** of **1011253** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

<phrase>(ring,oscillator) <sentence> <phrase>(process Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard
= Your access to full-text

---

1 **PCFL3: a low-power, high-speed, single-ended logic family**
Kanan, R.; Declercq, M.J.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 9 , Sept. 1999
Pages:1259 - 1269

[Abstract] [PDF Full-Text (360 KB)] **IEEE JNL**

---

2 **Spatial characterization of process variations via MOS transistor tin constants in VLSI and WSI**
Nekili, M.; Savaria, Y.; Bois, G.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 1 , Jan. 1999
Pages:80 - 84

[Abstract] [PDF Full-Text (112 KB)] **IEEE JNL**

---

3 **Process variation effects on circuit performance: TCAD simulation o 256-Mbit technology [DRAMs]**
Murthy, C.S.; Gall, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 16 , Issue: 11 , Nov. 1997
Pages:1383 - 1389

[Abstract] [PDF Full-Text (268 KB)] **IEEE JNL**

---

4 **Pseudo-complementary FET logic (PCFL): a low-power logic family i GaAs**
Kanan, R.; Hochet, B.; Declercq, M.;
Solid-State Circuits, IEEE Journal of , Volume: 31 , Issue: 7 , July 1996
Pages:992 - 1000

Brief Papers

Spatial Characterization of Process Variations via MOS Transistor Time Constants in VLSI and WSI

M. Nekili, Y. Savaria, and G. Bois

Abstract—**This paper is the first large-scale experimental characterization of spatial process variations for a parameter that is directly involved in timing issues: the MOS transistor time constant. This is achieved by measuring the oscillation period of high-speed (500 MHz) CMOS ring oscillators that are implemented at different locations on individual dies and over wafers. Novel phenomena are observed, improving our understanding of how process variations affect the performance of synchronous systems, particularly in clock distribution networks. We observed four components contributing to period variations: an environment-dependent component, a process-dependent component of lower spatial frequency, a random component analogous to white noise, and a component depending on the geometry of the power-supply distribution network.**

Index Terms—**Clock skew, MOS transistor, process variations, ring oscillators, time constant, wafer.**

I. Introduction

THE limitations due to fluctuations in process parameters have been anticipated at least since the 1970's [1]. To compensate for transistor mismatching, the design of high-precision analog circuits has been traditionally done by following a set of rules based on empirical knowledge acquired from experience [2]. With MOS technology scaling, mismatching in transistors has gained much more importance [3], particularly because process tolerances do not scale necessarily in proportion to geometries [4]. Indeed, miniaturization has been pursued very aggressively, and it is not clear that circuit tolerances have progressed accordingly. Moreover, it has been shown [5], [6] that the effects of process variations limit the accuracy of synchronization mechanisms in large integrated systems due to the quadratic growth of clock skew with respect to system size.

The need for a characterization of the process variations and its effects on timing parameters has been noted in the literature, especially in relation to large high-speed synchronous integrated systems [7]. To our knowledge, the only published work in this direction is due to Pavasovic *et al.* [8] and Andreou *et al.* [9]. Although their studies have provided a new insight into the "fine structure" behind transistor mismatch, the parameter used for such an exploration (the transistor drain current) does not directly characterize the timing performances. More recently, Gneiting and Jalowiecki [10] characterized process variations of timing parameters. However, no spatial correlation was established.

This paper is the first large-scale characterization of spatial process variations in a parameter that is directly involved in timing issues: the MOS transistor time constant. Variations of this parameter over large areas of silicon have direct consequences on the synchronization and timing performances of high-speed integrated systems. This characterization is achieved by measuring the oscillation period of high-speed (500 MHz) CMOS ring oscillators that are implemented at different locations on individual dies and on multiple wafers.

This paper is organized as follows. Section II describes the experimental device that was characterized. Section III presents an interpretation of the different spatial characterizations describing the process variations on die, from die to die, and from wafer to wafer. A privileged application of this paper is the design of clock distribution networks. However, the reported finding could have an influence on analog design methods and on the timing analysis in digital systems. Our findings and conclusions are summarized in Section IV.

II. Experimental Device

The spatial characterization presented in this paper is based on frequency measurements of a set of identical oscillators implemented at different locations on individual dies, as well as on dies distributed over a wafer. Since the sensitivity of synchronous integrated systems to process variations is expected to increase with the clock frequency, each oscillator consists of a chain of three minimum-sized inverters. Minimizing the number of stages gives the maximum frequency produced by this type of oscillator, and using minimum-size inverters makes parameter fluctuations linked to geometry variations substantial and more likely to be measurable.

To characterize the effect of process variations along the two dimensions, a test chip in the 1.2 μm Nortel CMOS technology was submitted to the Canadian Microelectronics Corp. (CMC). The test chip is composed of four separate segments of 20 oscillation cells each. To achieve the best spatial resolution in our characterization, the oscillation cells are kept at a minimal distance, which is determined by the geometry of the probe and the minimal distance required between passivation windows. This test chip is aligned along the borders of a die in a

Manuscript received April 17, 1997; revised May 11, 1998. This work was supported in part by the National Sciences and Engineering Research Council of Canada under Grant OGPOO06574 and in part by the Synergie program of the province of Quebec under a Grant.

The authors are with the Department of Electrical and Computer Engineering, VLSI Laboratory, Ecole Polytechnique de Montreal, Montreal PQ H3C 3A7 Canada (e-mail: nekili@vlsi.polymtl.ca).

Publisher Item Identifier S 0018-9200(99)00412-6.

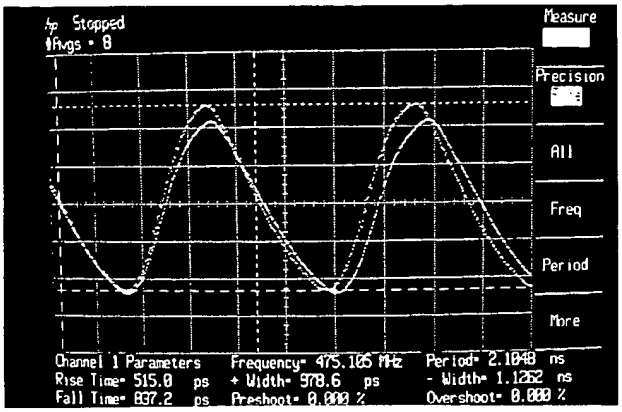

Fig. 1. Two signal outputs (photograph).

multiproject prototyping environment. This configuration has been adopted in order to minimize the partitioning of the die, whose core was used to implement the chips of other users. Each segment has independent power and ground buses to supply the oscillation cells from Vdd and Gnd pads. The die is 1.44 × 1.44 cm^2, and the wafer contains 55 dies.

Experiments were first performed on ten different dies from an initial wafer returned by the CMC, and then two other wafers were requested in order to perform characterizations in wafer scale integration (WSI). The frequency measurements were repeatable within 10 ps of the clock period. Also, a jitter between 60–190 ps was experienced with the probed signal. For complete details about this experiment, see [11].

III. Discussion of Experimental Results

Early experimental results showed a good match with HSPICE simulations. Fig. 1 shows the measured output signal of two typical oscillation cells, with a peak-to-peak voltage of 163 and 190 mV, and respective clock frequencies of 500 and 475 MHz.

At the die level, a characterization of the clock period for oscillators implemented on the four sides of a die is shown in Fig. 2. All data analysis and plotting in this section are produced using MATLAB [12]. Depending on the location of the oscillator within the die, the oscillation period varies between 1945 and 2670 ps, which represents a measured variation of 37% between minimum and maximum values. This is a substantial variation that can affect seriously the synchronization of a high-performance chip if it was experienced by buffers in a clock tree.

Observations of the clock period at a wafer scale revealed local and global effects in addition to "white noise." The nature of surrounding devices (environmental component) seems to profoundly shape the time constant of active devices, and large-scale variations (process component) show pronounced "edge" effects capable of drastically reducing the worst case performance of chips. A spectral analysis over 100 cells in both X and Y directions has been performed in [11], thus confirming the presence of these local and global effects. Also, the geometry of the power-supply distribution network plays a significant role.

A. The Environmental Component

A pattern of period variations seems to repeat itself throughout the wafer. Fig. 3 shows the variations of clock period along five adjacent dies in the X and Y directions for one of two nonscribed wafers considered in the experiment. Measured periods of 20 cells per die (one side) are represented in both directions. One can clearly notice the "periodicity" of the clock period values with the position in both directions. An intuitive *a priori* explanation of such a periodicity is proposed in the following. If we recall that inside the die, several unrelated designs of other users are implemented in a multiproject fabrication run, it becomes clear that the electrical environment along a given die side varies when we move from end to end. However, since it is obvious that oscillation cells located at the same position in all dies have identical electrical environments (dies are replicated over the wafer), moving along an orthogonal direction such as the X-axis or Y-axis, over more than one die, lead to the same environment every 20 cells (total number of cells implemented along one die side). Indeed, the clock period behaves as if it were modulated or shaped by the electrical devices in the immediate environment of the oscillation cells along the die side. However, it tends to return to approximately the same value every 20 positions, and the sudden increases and decreases happen approximately at the same positions within the period over the five die sides.

Consequently, interpolating the internal regions from the die borders, which might have different electrical environments, seems to be infeasible in presence of an environmental component of this nature and magnitude.

With current design strategies, the presence of the environmental variation described above seems to be inevitable. Indeed, it is intrinsic to the fact that a clock distribution network, for instance, is always surrounded by the logic it feeds. The clock period "periodicity" mentioned earlier leaves little doubt about the direct influence of environment variability on the time period of oscillation cells. Since each cell faces a region with different electrical characteristics, depending on which electronic devices a designer implements in the surroundings of a clock distribution network, some regions of the tree will be faster than others. Note that even though a chip designer has the knowledge of the nature and position of the devices he implements, the effect of these devices on the close neighbor active logic of the clock distribution network, when fabricated under a real manufacturing process, remains unknown. In this paper, this effect is called the "environment" phenomenon.

B. The Process Component

The behavior of the clock period variations cannot be explained just by environment-related dependencies coupled to low-amplitude "white noise." Indeed, a second component can be observed from Fig. 3. This component varies according to the location of the oscillation cell on the wafer. It can be easily noticed, for example, from the varying amplitude of the maximal peak within a die side, along X and Y directions. This type of variation is probably due to large-scale

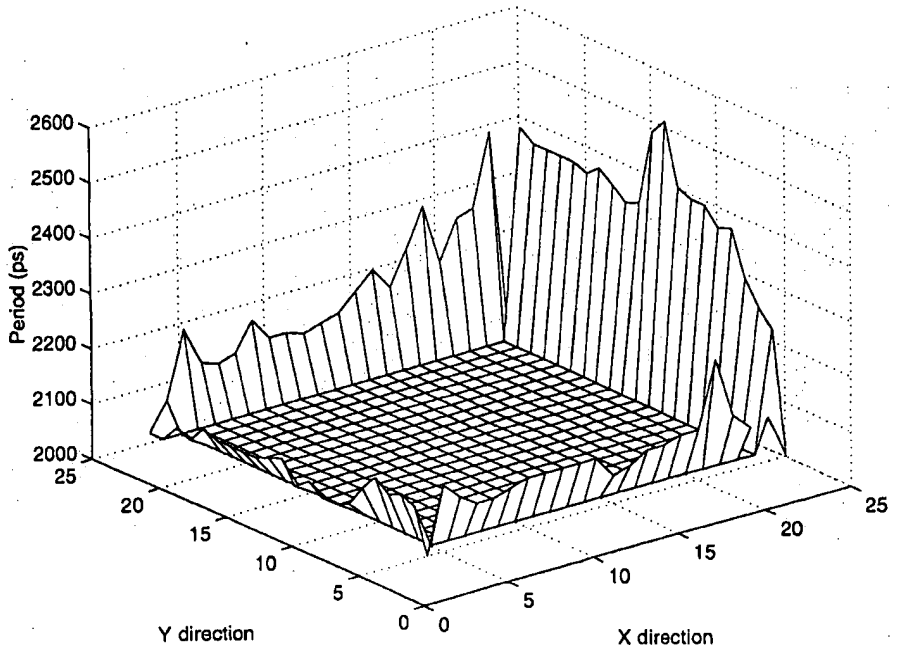

Fig. 2. Four-side representation of clock period at the die level.

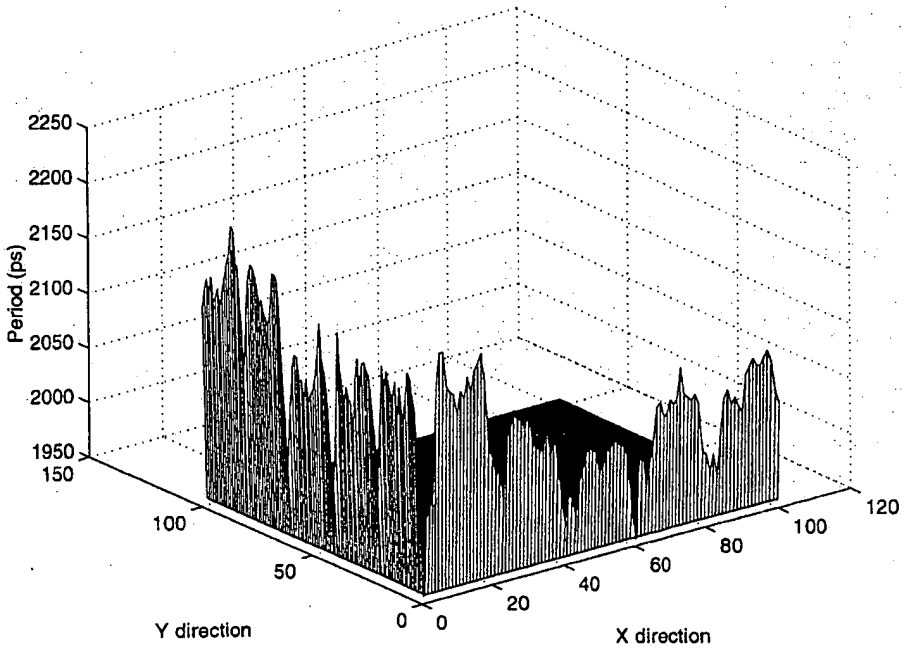

Fig. 3. Correlation along X and Y directions.

nonuniformity in the process (variations in transistor threshold, transistor channel length, and width over long distances).

This large-scale component is shown in Fig. 4 (for one of the two nonscribed wafers considered in the experiment), where a single oscillation cell, the same, is considered in all dies in order to keep the environment constant. Fig. 5 provides in a tabular format the data used in Fig. 4. According to these data, in most cases, cells in regions of higher logic densities seem to produce lower clock periods than the cells facing open areas (cells corresponding to numbers in bold in Fig. 5). Also, a dominant peak in the oscillator period is observed in the middle region of the wafer's left border. That region corresponds to a location at which the wafer appears stressed, probably due to mechanical wafer manipulation. Color changes were clearly noticeable on both the left and right sides of the wafer. If no spatial criteria are established for considering dies for subsequent tests, a die implemented in such regions of the wafer might pass the test and affect substantially the worst case

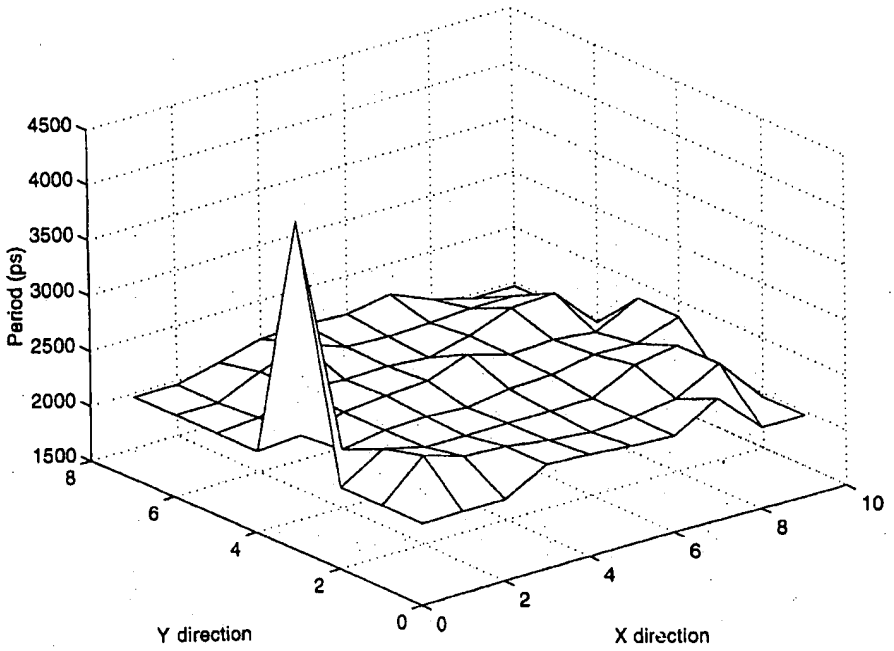

Fig. 4. Spatial characterization of clock period on WSI scale.

1938	1938	**2482**	2185	2179	2197	2164	**2349**	1938	1938
1938	**2402**	2186	2211	2237	2206	2169	2137	**2331**	1938
1938	**2448**	2268	2184	2171	2149	2188	2181	**2209**	1938
2295	2166	2148	2160	2148	2156	2169	2248	2140	**2290**
3485	2142	2145	2170	2150	2368	2177	2216	2181	**2194**
1938	**2329**	2125	2154	2101	2153	2135	2161	**2168**	1938
1938	**2321**	2085	2155	2151	2138	2117	2143	**1938**	1938
1938	1938	**2230**	2087	2137	2183	2100	**2000**	1938	1938

Fig. 5. Numerical values of the clock period (in ps) as measured at the same position in respective dies. It clearly illustrates the existence of a process component. (Note: since the wafer is not rectangular, inexistent dies have been replaced by the minimal period value, i.e., 1938 ps.)

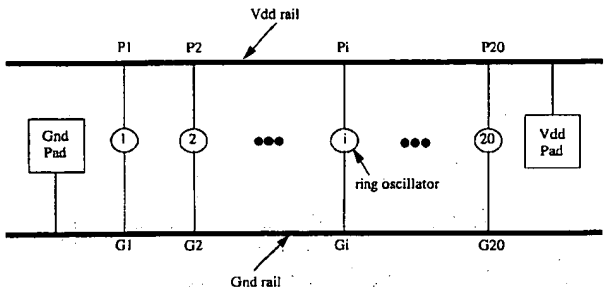

Fig. 6. Schematic of the power-supply distribution network.

performance of a chip design implemented with the considered technology. This observation is significant, since very-large-scale integration (VLSI) parts are usually designed to meet a target specification with worst case process parameters. Our results indicate that the location of worst case process parameters may be predictable.

C. The Power-Supply Component

A segment of ring oscillators can be modeled according to the schematic in Fig. 6. In our experiment, the power signals Vdd and Gnd were supplied via dc probes and pads located at the ends of the segment, and then distributed to the ring oscillators through parallel rails. As a consequence, each ring oscillator inherits a pair of local power supplies, noted (Pi, Gi), $i \in [1, 0]$. The distance between two adjacent ring oscillators in our test design is approximately 0.7 mm. This experimental setup introduces the possibility of ohmic voltage drop between the oscillators. Indeed, HSPICE [13] electrical simulations showed that power-supply fluctuations take place along the Vdd rail as well as along the Gnd rail. These fluctuations constitute a significant portion of the total variations. Note that this type of clock period variation component depends solely on the geometry of the power-supply distribution network and should be considered in the circuit design phase. It manifests itself as a variable current along the power-supply rails. Due to the resistance between ring oscillators, the variable current induces a variable voltage that directly modulates the clock period. In a typical VLSI or WSI circuit, this current varies with the power consumption in the various parts of the chip and with time, since the activity that directly governs the power consumption in CMOSalso varies.

Based on the quasi-random phenomena observed in environmental, process, and power-supply components, the effectiveness of some conventional techniques to compensate for process variations [14] becomes questionable. For instance, a recent attempt using such techniques [15] aimed at constructing a clock distribution tree by sizing separately PMOS and NMOS transistors. Shoji's technique [14] assumes that all PMOS transistors (on which the buffers of the clock tree are based) are subject to the same type of process (fast, slow, or typical). The same was assumed to apply to NMOS transistors. However, the characterization performed

in this paper shows that active devices, such as inverters, are subject to large dispersions in their time constants depending on the position of the transistor in the wafer and on the nature of its surroundings. As a consequence, only a small proportion of the transistor population is close to the worst or best case. Therefore, designing a clock system based on transistor worst case performance will cause a substantial penalty to the clock frequency, whereas in practice, one might take advantage of the variations of transistor performance throughout the wafer.

IV. Conclusion

In this paper, we have presented the first large-scale experimental characterization of spatial process variations on a parameter that is directly involved in timing issues: the MOS transistor time constant. This is achieved by measuring the oscillation period of high-speed (500 MHz) CMOS ring oscillators that are implemented at different locations on individual dies and over wafers.

An environmental phenomenon that modulates the clock period was observed. That phenomenon manifests itself as a strong periodic influence due to variations in surrounding electrical devices. It can be viewed as a generalization of the "edge" effect observed and reported in previous work. Also, a large-scale process component induces shifts into the environmental part of the period variations. This component is characterized by a much lower spatial frequency. Based on their measurements, Gneiting *et al.* assumed in [10] that on-wafer variations are negligible. Due to new phenomena that we observed, their assumption appears to be very questionable, not only at wafer scale but particularly at die level. Similarities can be drawn between the "striation" effect observed by Pavasovic *et al.* [8] and Andreou *et al.* [9] with the environmental component (in terms of "periodicity") as well as between the "gradient" effect and the process component (in terms of low frequency). Also, important "edge" effects were observed on the wafer borders. The effects of the power-supply distribution network on the clock period variations were analyzed and proved to be significant.

Acknowledgment

The authors would like to acknowledge Prof. J. Currie for making available the facilities of the LISA laboratory, N. Gravel for his helpful experience in wafer probing, and A. Rahal from POLY-GRAM laboratory for helpful discussions on microwave issues, all at the Ecole Polytechnique of Montreal. The authors also acknowledge the Canadian Microelectronics Corp. and Nortel for manufacturing their experimental device and for providing full wafers for testing.

References

[1] R. W. Keys, "Physical limits in digital electronics," *Proc. IEEE,* vol. 63, no. 5, pp. 740–767, 1975.
[2] E. A. Vittoz, "The design of high-performance analog circuits on digital CMOS chips," *IEEE J. Solid-State Circuits,* vol. SC-20, no. 3, pp. 657–665, 1985.
[3] M. J. Pelgrom, A. C. J. Kuinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits,* vol. 24, no. 5, pp. 1433–1440, 1989.
[4] E. H. Li and H. C. Ng, "Parameter sensitivity for narrow-channel MOSFET'S," *IEEE Electron Device Lett.,* vol. 12, pp. 608–606, Nov. 1991.
[5] A. L. Fisher and H. T. Kung, "Synchronizing large VLSI processor arrays," *IEEE Trans. Comput.,* vol. C-34, pp. 734–740, Aug. 1985.
[6] M. Nekili, G. Bois, and Y. Savaria, "Pipelined H-trees for high-speed clocking of large integrated systems in presence of process variations," *IEEE Trans. VLSI Syst.,* vol. 5, pp. 161–174, June 1997.
[7] E. G. Friedmann, *Clock Distribution Networks in VLSI Circuits & Systems.* New York: IEEE Press, 1995, ch. 1.
[8] A. Pavasovic, A. G. Andreou, and G. R. Westgate, "Characterization of subthreshold MOS mismatch in transistors for VLSI systems," *J. VLSI Signal Process.,* vol. 8, pp. 75–85, June 1994.
[9] A. G. Andreou and K. A. Boahen, "Neural information processing II," in *Analog VLSI,* M. Ismail and T. Fiez, Eds. New York: McGraw-Hill, 1994.
[10] T. M. Gneiting and I. P. Jalowiecki, "Influence of process parameter variations on the signal distribution behavior of wafer scale integration devices," *IEEE Trans. Comp., Packaging, Manufact. Technol. B,* vol. 18, pp. 424–430, Aug. 1995.
[11] M. Nekili, "Synthesis of clock distribution networks in presence of process variations," Ph.D. dissertation, Ecole Polytechnique de Montreal, Montreal, Canada, May 1998.
[12] MATLAB, "High-performance numeric computation & visualization software," reference guide, MATH WORKS, Inc., MA, 1992.
[13] *HSPICE User's Manual,* Meta-Software, Inc., CA, 1992.
[14] M. Shoji, "Elimination of process-dependent clock skew in CMOS VLSI," *IEEE J. Solid-State Circuits,* vol. SC-21, pp. 875–880, 1986.
[15] J. G. Xi and W. W. M. Dai, "Buffer insertion and sizing under process variations for low power clock distribution," in *Proc. 32nd Design Automation Conf.,* 1995, pp. 491–496.